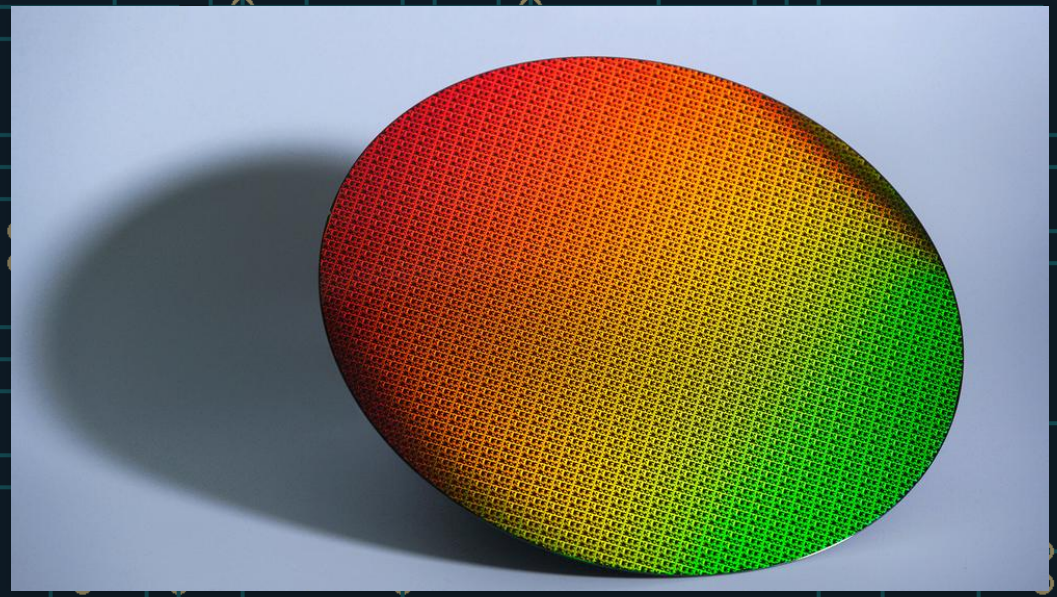
UNIVERSITY OF COLORADO BOULDER // OCTOBER 2026

Chiplet Talk

Chiplets, Advanced Packaging, and the Chips Behind AI



Judd Gerber
Sort/Test Technology Development, Intel

Introduction – Judd Gerber

- Senior Principal Engineer in Sort/Test Technology Development at Intel
- Worked in Semiconductor Test for over 30 years
- Currently manages Sort Development for Intel
- Electrical Engineering Degree from University of Idaho
- Enjoys Fly Fishing in Spare Time



Rainbow trout released back to the Kvichak River, SW Alaska

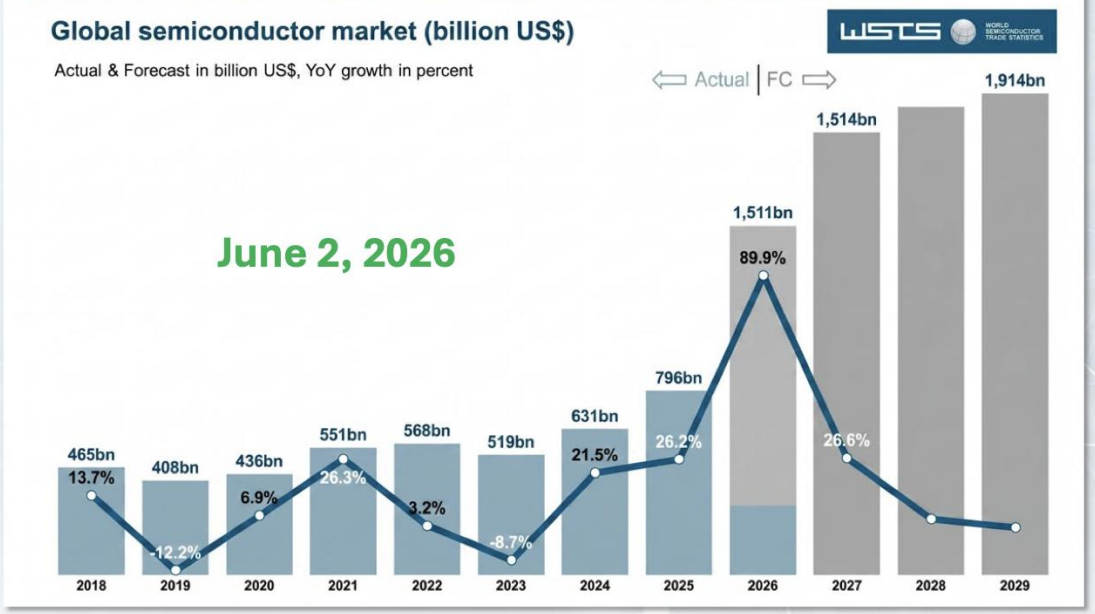
Why Is Everyone Talking About AI?

Unprecedented Growth | AI Era

35th ANNIVERSARY

2026: Semiconductor Market Surpasses USD 1.5 Trillion Driven by Extraordinary Memory Expansion

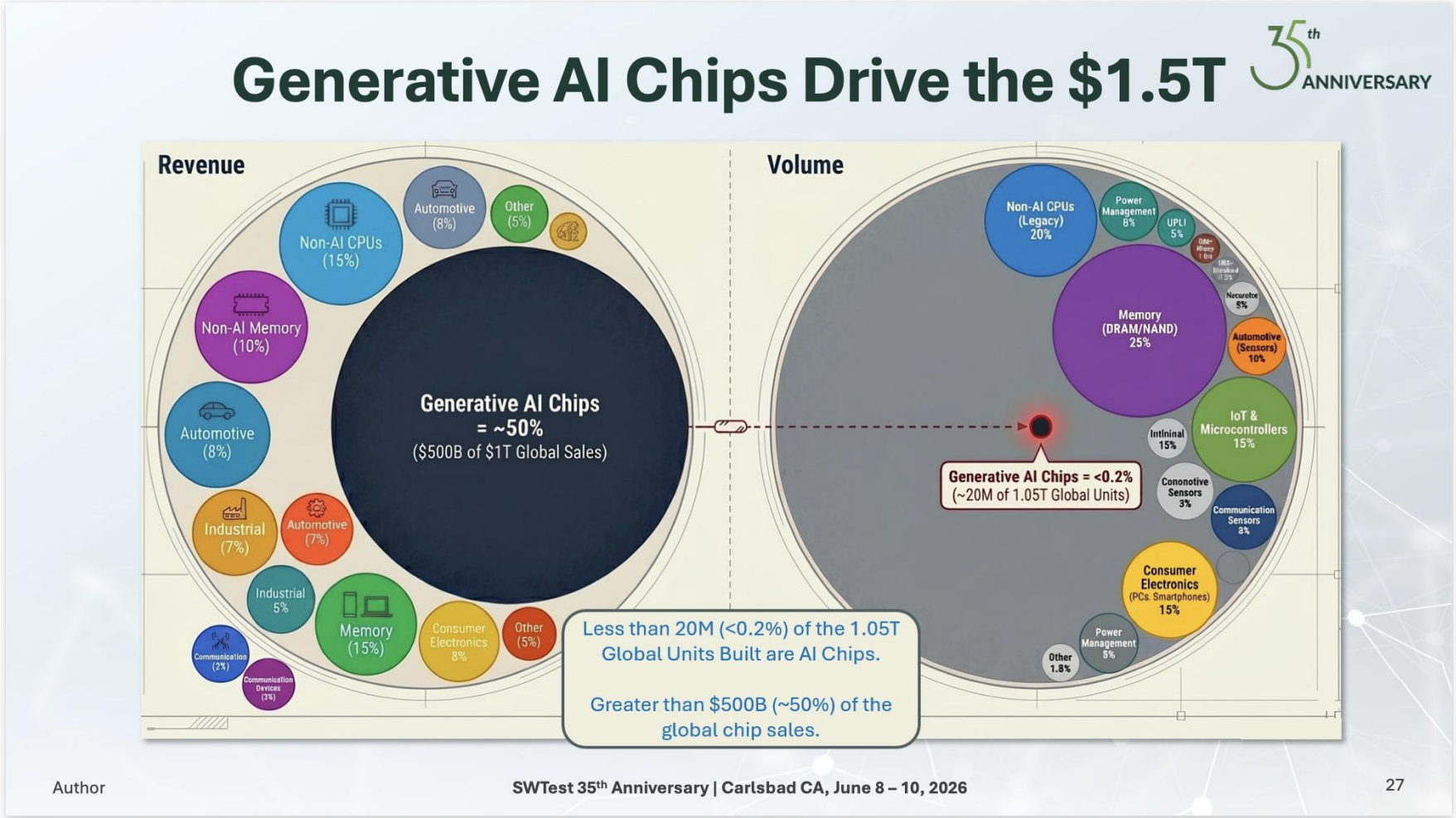
Following exceptionally strong results in late 2025 and early 2026, the global semiconductor market is now projected to grow 90 percent in 2026, reaching USD 1.51 trillion.



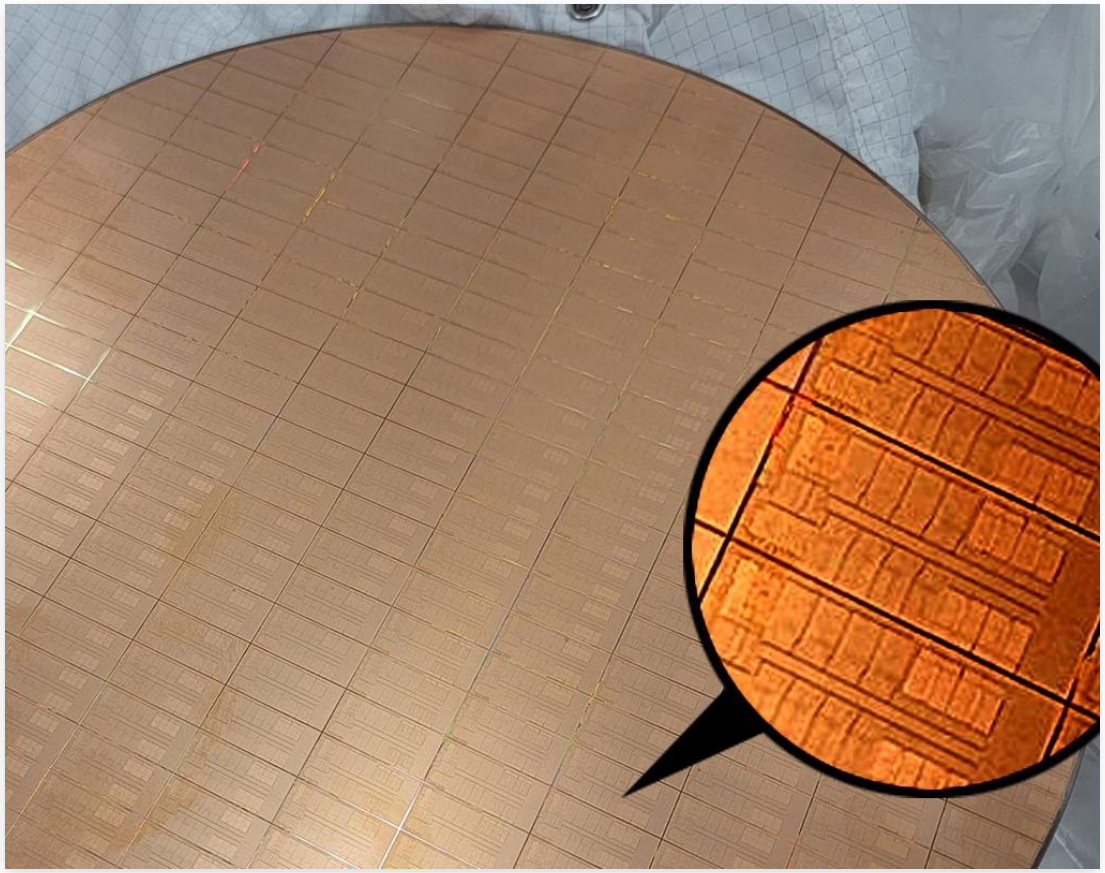
J. Broz

SWTest 35th Anniversary | Carlsbad CA, June 8 – 10, 2026

Why Chiplets and Advanced Packaging Matter Now



What Do Die and Wafers Look Like?



This is a 300mm Intel wafer. The Die are "Diced" or cut along the lines you see on the wafer between the Die.

What is a Chip?

A Chip (microchip, computer chip, or integrated circuit) is a set of circuits designed into a functioning unit and built on a round silicon wafer.

What is a "Die?

A Die is a Chip before it is packaged. It could be in wafer form or an individual unit after the wafer has been "Cut Up" or "Diced".

300 mm

wafer diameter – current state of the art

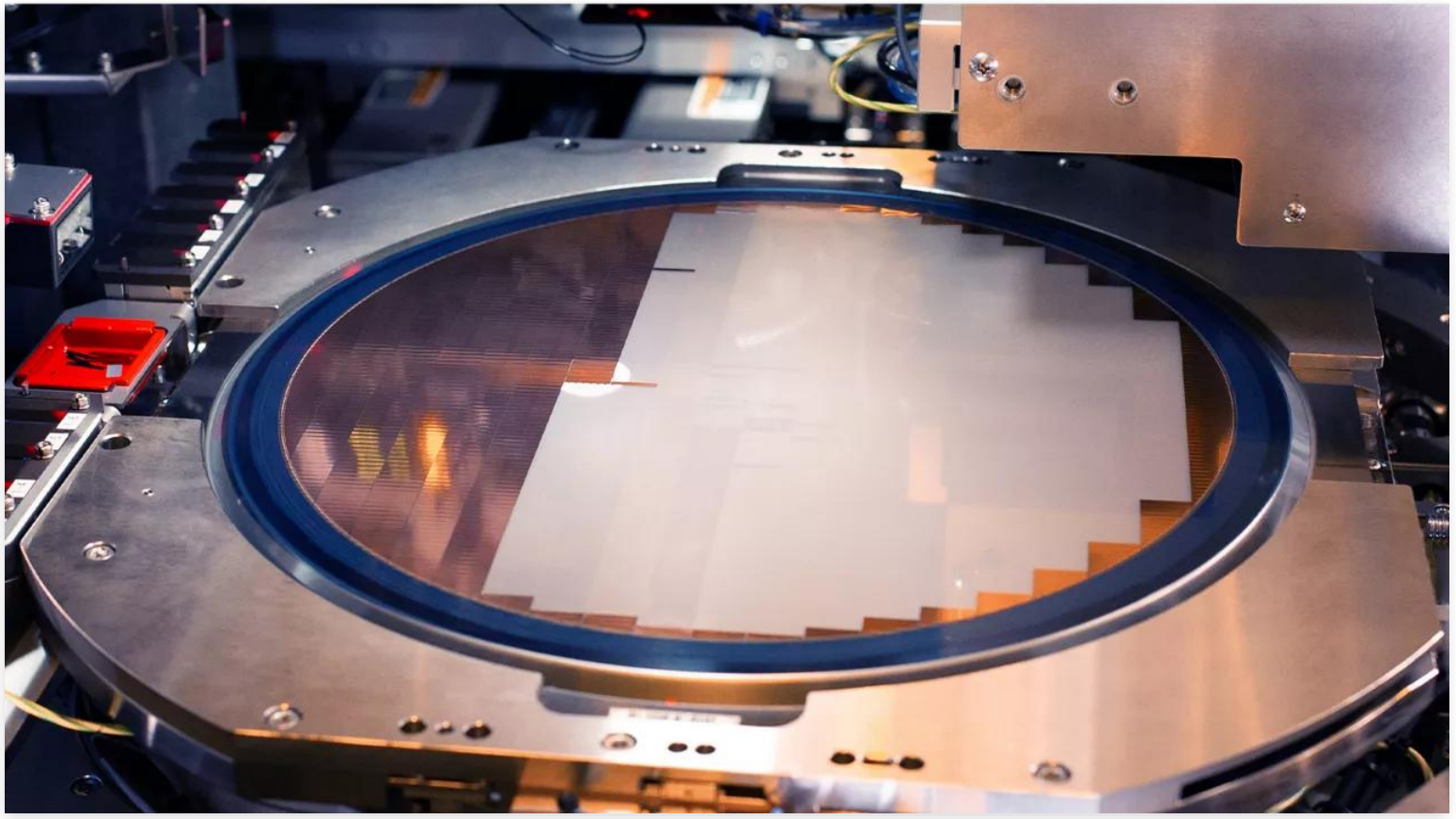
257 mm²

area of each die

~275

die on one 300mm wafer

Dicing and Picking the Die

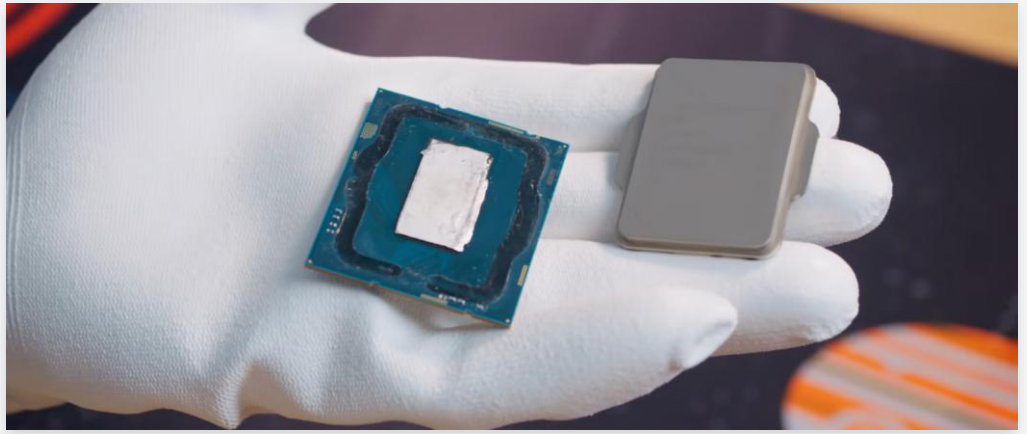


This is a wafer that has been “Diced” and the individual Die are being “Picked” from the wafer to be placed in packages.

What Do Packaged Die or Chips Look Like?



This is an Intel Microprocessor Chip packaged for a Desktop Computer application.



The same Chip with the Lid or Integrated Heat Spreader (IHS) removed. Note the Die is covered with white Thermal Interface Paste.

This is a “Simple Package” with only one Die per Package.

Simplified Semiconductor Manufacturing Flow

01

Wafer Fabrication

Making the Wafer

02

Sort

Electrically Testing the Die on the Wafer

ELECTRICAL TEST

03

Die Preparation

Cutting up or dicing the Wafer into individual units to be packaged

04

Packaging

Soldering the Die into a package to create a Chip, which is the Final Product

05

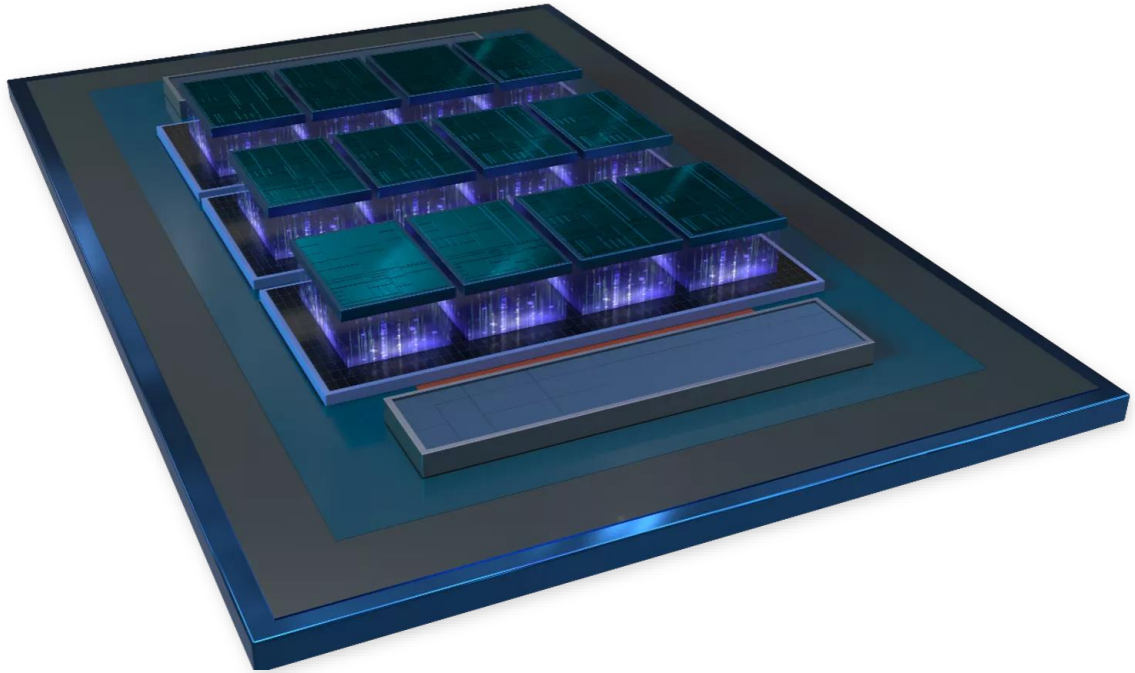
Final Test

Electrically Testing the Packaged Chip Final Product

ELECTRICAL TEST

What Is a Chiplet?

Chiplets are small modular integrated circuits (ICs) designed to function as components of a larger chip.



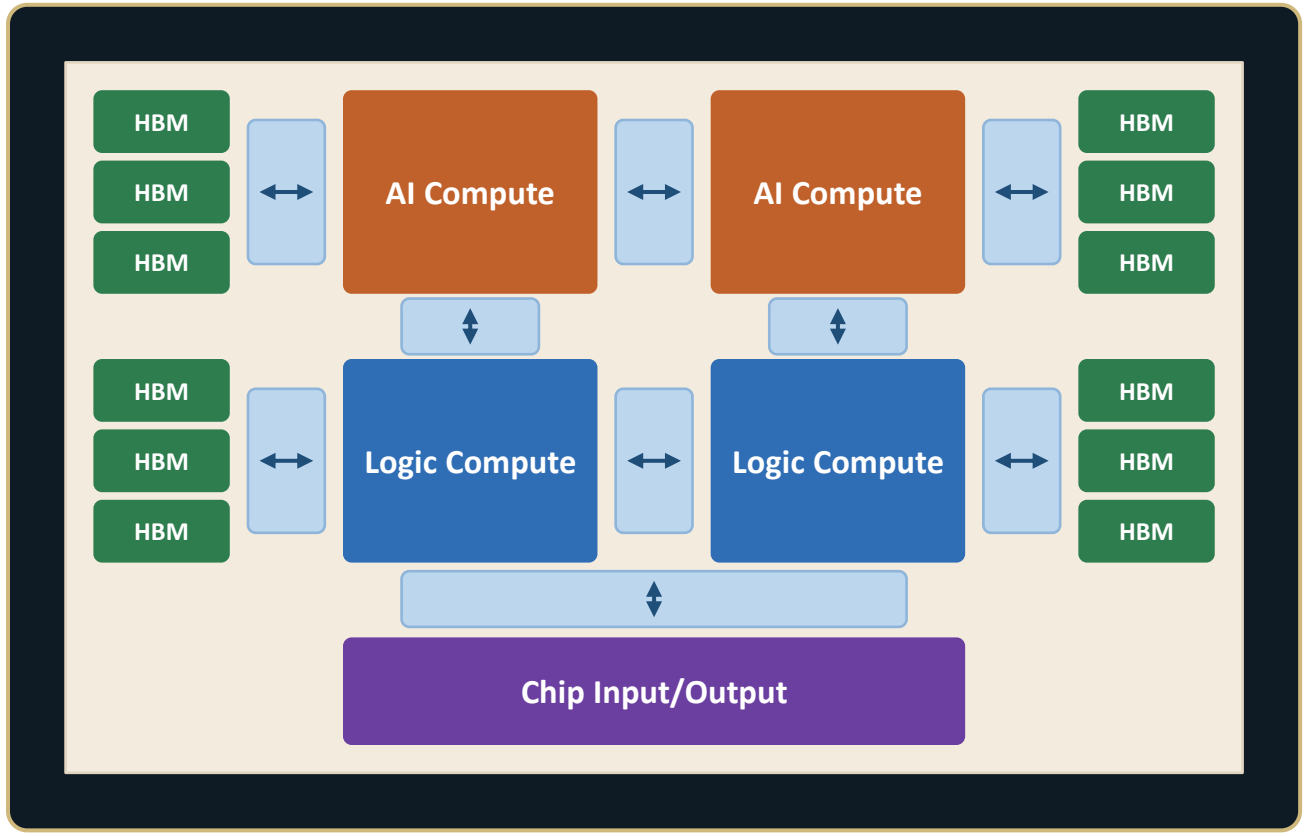
Example AI Chip

AI Compute Chiplets
Use Computer Graphics Processing Unit (GPU) like Architecture.

Logic Compute Chiplets
Use Computer Central Processing Unit (CPU) like Architecture.

HBM Chiplets
"High Bandwidth Memory" to support all the on-chip computing.

Input/Output Chiplet
Interface to external devices through standard compute interfaces like PCI and Serializer/De-Serializer (SerDes) for Optical Interconnect.



Summary: Many different Chiplets of different types are integrated together to make one AI Chip.

Why Can’t We Make a Single-Die AI Chip?

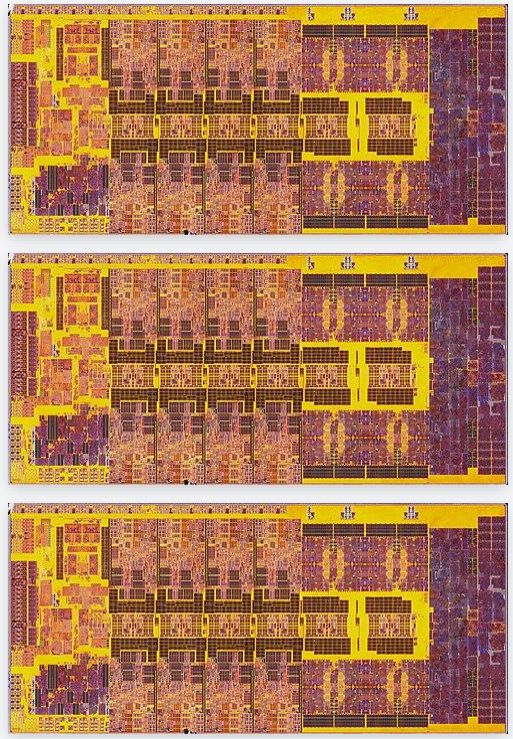
Lithography is a Hard Technical Limitation

- Lithography is shining light through a patterned mask to create circuits on a wafer.
- The max size of mask that we can make today is ~850mm².

Problem
For the die from earlier, we can only fit 3 “compute” die in 1 mask.

Solution
We need to break the Die into smaller Chiplets.

ONE MASK ≈ 850 mm²



257 mm²
This is the Die from earlier

3 × 257 = 771 mm²
A 4th die won’t fit

Chiplets Enable Modular Designs

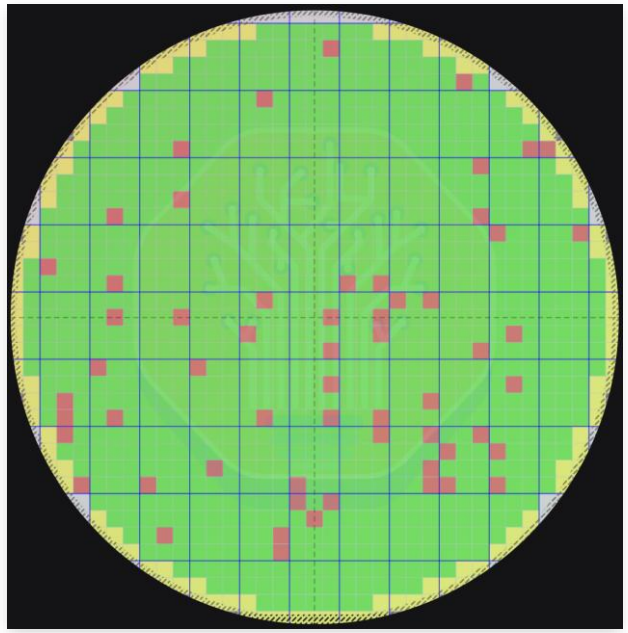
	Chiplet	Single Chip
Design reuse	✓ Reuse proven circuits / chiplets from previous designs.	✗ Any circuit change requires all new masks and validation for a “new” chip.
Upgrades	✓ Can upgrade individual chiplets – Example: Faster memory.	✗ Any circuit change requires all new masks and validation for a “new” chip.
Supply chain	✓ Can dual-source chiplets to help with supply chain issues.	✗ N/A – The entire chip would have to be dual-sourced.
Fab process	✓ Each chiplet can be made on its own optimized fab process.	✗ The entire chip must be made on the most expensive fab process.

Chiplets Enable Better Yields and Lower Cost

Chip Cost is driven by the cost of making the wafer – the more area on the wafer that you can use, the lower your cost.

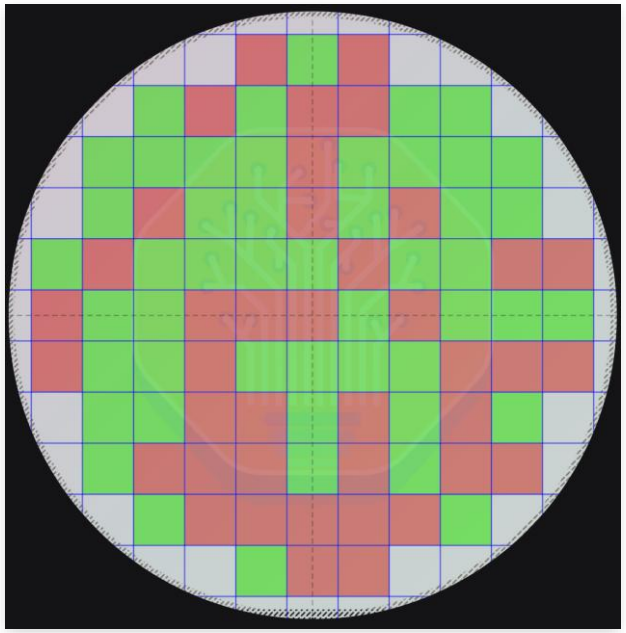
Smaller Die better utilize the available area.

Smaller Die are better for Yield.



19%

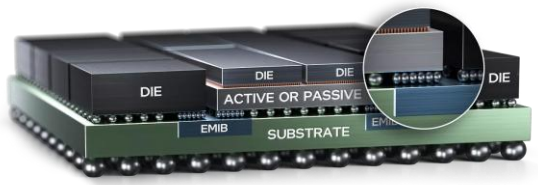
Small Die: wasted area



57%

Large Die: wasted area

Chiplets Enable Advanced Packaging and AI Chips



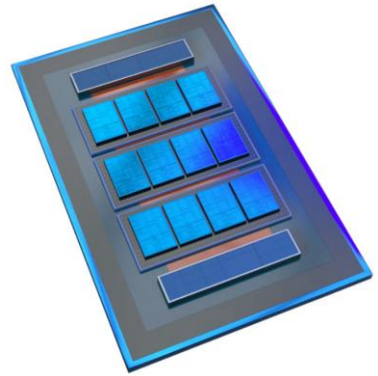
Intel EMIB

Advanced Packaging - Embedded Multi-die Integrated Bridge



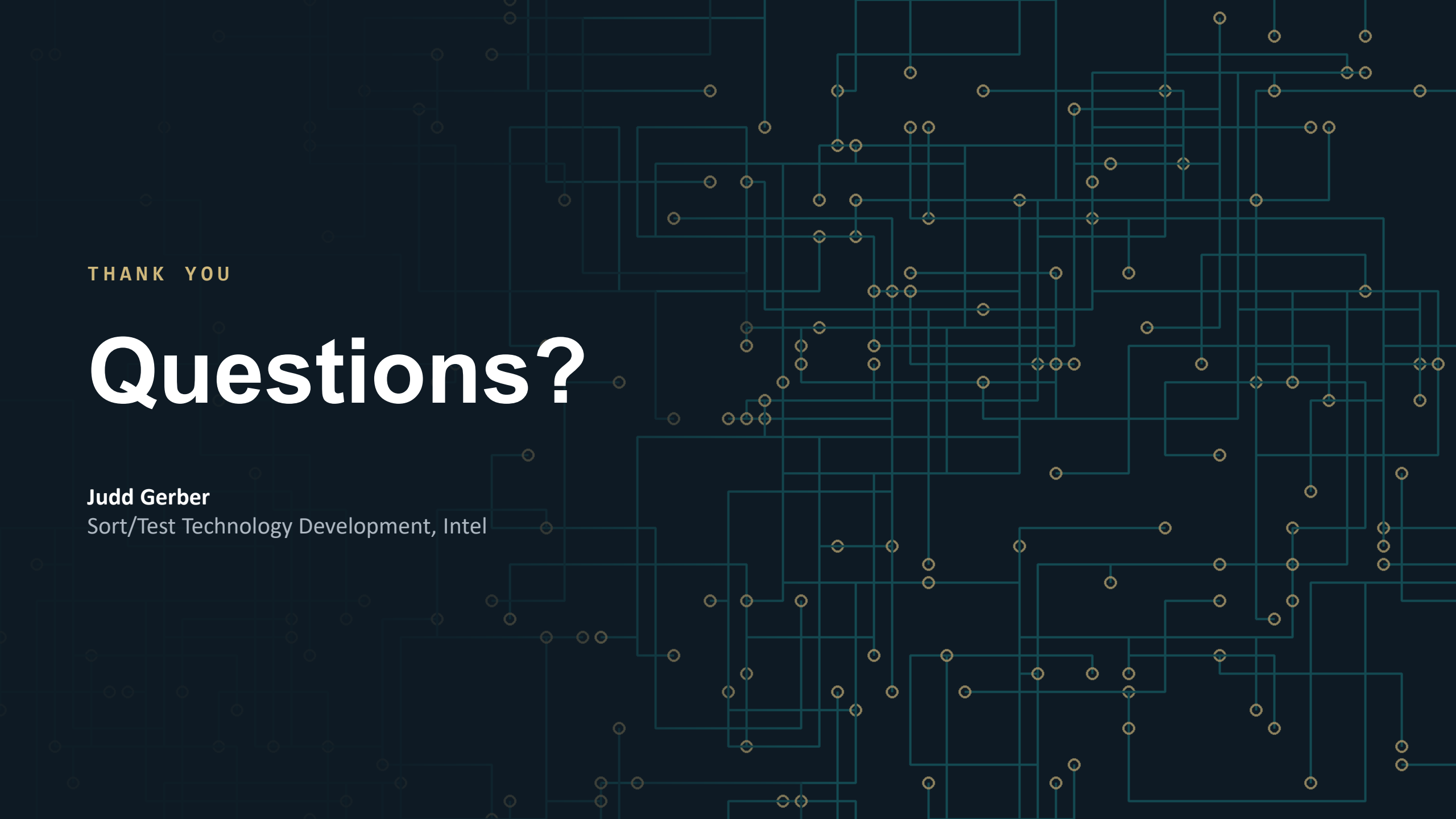
Intel Foveros Direct

Advanced Packaging – Hybrid Bonding Interconnect (HBI)



Clearwater Forest

An Intel product code named Clearwater Forest, which uses both Foveros Direct and EMIB.



THANK YOU

Questions?

Judd Gerber
Sort/Test Technology Development, Intel