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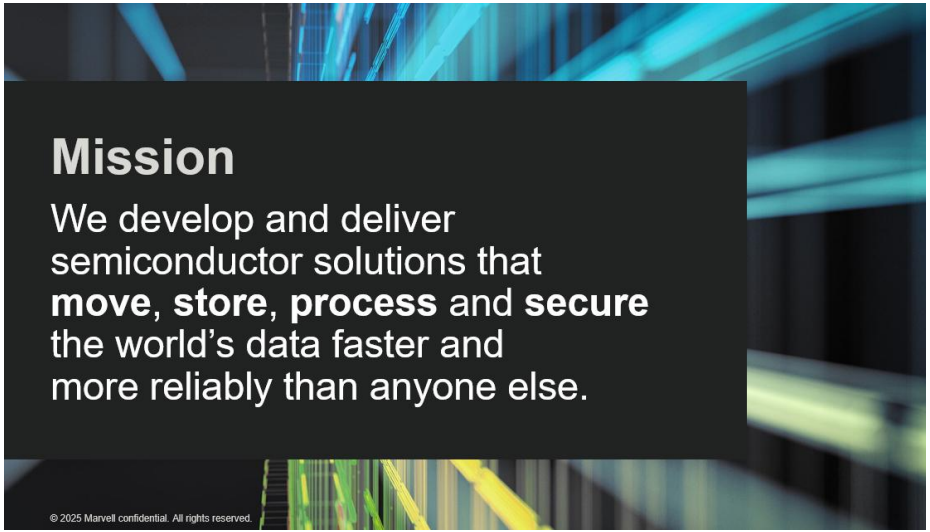
Advanced Semiconductor Packaging

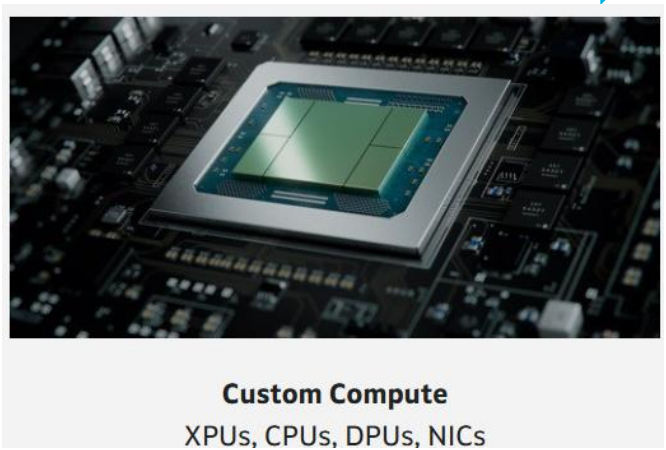
The New Epicenter of Innovation

Chris Fieldsend
Director, Advanced Packaging

A bit about Marvell

- Fabless Semiconductor Company
- Established 1995
- 10,000+ employees among world-wide design centers
- Hyper-growth through organic hiring & strategic acquisitions
- 2025 record revenue of ~$8.2billion, up 42% year-over-year





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AGENDA

What We'll Cover

01 **A Brief History of Package Evolution**

From through-hole DIPs to wire bond, flip chip, and today's 2.5D/3D heterogeneous integration

02 **Why Packaging Became a First-Order Design Problem**

Moore's Law economics, reticle limits, and the shift from transistor scaling to system scaling

03 **The Package Design Menu**

Wire bond, flip chip (FCBGA), fan-out (FOWLP), 2.5D interposer, 3D stacking, and chiplets

04 **Signal Integrity (SI) Context**

Why each package type exists from a loss, reflection, and bandwidth-density standpoint

05 **Power Integrity (PI) Context**

PDN impedance, IR drop, and decoupling strategy for each architecture

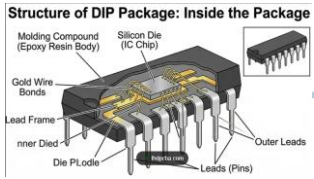
06 **Advanced Packaging at Marvell**

How custom silicon and data infrastructure products apply these choices

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HISTORY

The Evolution of Semiconductor Packaging



1960s–70s

Through-Hole DIP

Die wire-bonded inside a ceramic or plastic body; through-hole pins soldered into the PCB

Photo credit: www.electronicsandyou.com

<40 leads
<30MHz
L= 5-35nH
Ground Bounce (SSN)



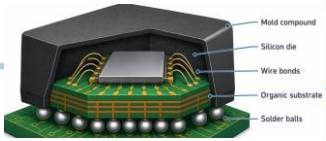
1980s

Surface Mount (QFP / SOIC)

Gull-wing leads soldered flat to the board surface; smaller footprint, higher lead count

Photo credit: www.digikey.com

<240 pins
<100MHz
IR drop (thin leads),
Higher SSN (fast switching),
Crosstalk (thin, dense, co-planer)



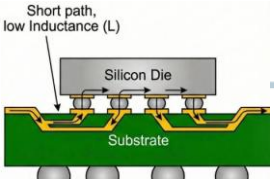
1990s

Ball Grid Array (BGA)

Perimeter leads replaced by an area array of solder balls; shorter paths, far more I/O

Photo credit: www.pcbcool.com

<240 pins
<200MHz
Transmission line effects: (EM solver req'd)
3D substrate Routing (VIA inductance)
Impedance discontinuities
Crosstalk (fine pitch routing, BGAs)
Insertion Loss (early laminates)



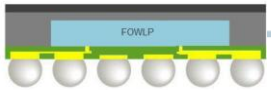
1990s–2000s

Flip-Chip (C4)

Die flipped face-down onto solder bumps; wire bonds eliminated for lower inductance

Photo credit: www.jlcpcb.com

Hundreds MHz-GHz
Eliminated bond wires
High insertion loss (skin effect at high freq)
Requires S-parm simulation
Xtalk becomes major design problem (density)
PI becomes "a thing" in pkg
- Low L by eliminating leads
- IR drop requires significant design considerations as far greater current through denser connections/plans
- High di/dt (Inrush current)



2010s

Fan-Out Wafer-Level (FOWLP)

Redistribution layers fan I/O out beyond the die edge, no substrate required

Photo credit: 3dfabric.tsmc.com



2.5D/3D Heterogeneous Integration

Multiple dies (logic + HBM) bridged via a silicon interposer (CoWoS) or embedded silicon bridge (EMIB) for massive bandwidth

Full system integration
6K+ BGAs
Compute <> Memory in pkg
Multi-TB/s memory bandwidth
Co-package network switching
IO, Security

Extreme fine pitch interconnect
Mixed dielectrics in same path
High speed Die-to-die
Heat/Variable resistivity
Complex PDN – D2D coupling

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MOTIVATION

Why Packaging Became a First-Order Design Problem

Transistor scaling alone no longer delivers the performance-per-watt and bandwidth density that AI, networking, and storage silicon require. Packaging has moved from a low-cost commodity step to a primary lever for system performance.

Reticle & Yield Limits

Max die size is fixed by lithography (~858 mm²). Bigger systems require multiple die stitched together in package, not on one die.

Memory Bandwidth Wall

CPUs/XPUs are starved for bytes/FLOP. Off-chip DRAM (DDR) can't supply the bandwidth AI workloads need at reasonable power.

Cost of Monolithic Scaling

Leading-edge wafer cost grows faster than die shrink saves money. Splitting a design into chiplets on cheaper nodes cuts cost per function.

Heterogeneous Integration

Optimal SoCs mix process nodes (logic, analog, RF, memory, optics). No single silicon process is best for every function.

Power Delivery & Thermals

Shorter interconnects reduce I/O energy per bit; stacking concentrates heat, and PDN design must keep pace with die-to-die density.

Time-to-Market / Reuse

Proven chiplets (SerDes, compute, I/O) can be re-combined across products instead of re-designing a monolithic die each time.

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PACKAGE DESIGN OPTIONS

The Modern Packaging Menu

There is no single “best” package — each option trades cost, interconnect density, electrical performance, and thermal capability differently. Design teams select the architecture that matches the product's bandwidth, power, and cost targets.

Package Type	Key Electrical Trait	Typical Use Case
Wire Bond BGA	Lowest cost, mature, moderate I/O	Cost-sensitive, lower-speed logic
Flip Chip (FCBGA)	Low inductance, high I/O, good thermal	High-performance SoCs, networking ASICs
Fan-Out WLP (FOWLP/InFO)	Thin, no substrate needed, fine RDL	Mobile, compact multi-die SiP
2.5D Interposer (HBM-class)	Ultra-fine die-to-die wiring, enables HBM	AI accelerators, high-BW switch ASICs
3D Stacking (TSV / Hybrid Bond)	Highest density, shortest vertical links	HBM cube stacks, cache-on-logic
Chiplets / Multi-Die (organic or interposer)	Mix nodes, reuse IP, standardized D2D PHY	Modular custom silicon platforms

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PACKAGE TYPE

Wire Bond BGA / CSP

WHY IT EXISTS

The workhorse of low-to-mid-cost packaging. Fine gold or copper wires connect die pads directly to substrate fingers — no bumping step, mature equipment base, and tolerant of die-to-substrate size mismatch. Still the default for cost-sensitive logic, sensors, and analog.

SI CONTEXT

Bond wires are long (1–3 mm) and inductive (~0.5–1 nH/mm). This inductance dominates high-frequency return loss and limits usable bandwidth — fine for lower speed I/O, but a hard ceiling for multi-Gb/s SerDes without careful wire-length matching and ground-wire interleaving.

PI CONTEXT

Power and ground also ride on inductive bond wires, so di/dt switching noise creates larger simultaneous-switching noise (SSN) than flip chip. Designers add multiple parallel ground/power wires per pin and rely on package/board decoupling capacitance to hold the PDN impedance flat.

0.5–1 nH/mm
Bond wire inductance

Low
Relative unit cost

<3–5 GHz
Practical I/O ceiling

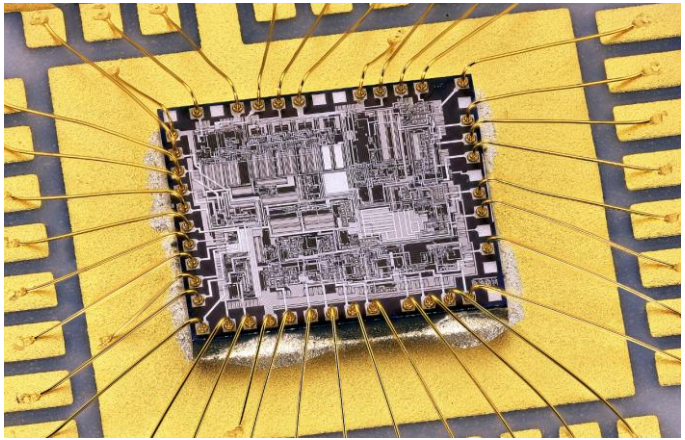


Image credit: Mister rf - Own work
07R01 IF Amplifier/Demodulator Integrated Circuit Motorola GM350 transceiver

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PACKAGE TYPE

Flip Chip (FCBGA)

WHY IT EXISTS

The die is flipped face-down and connected to the substrate through an array of solder “micro-bumps” spread across the whole die surface, not just its perimeter. This unlocks far higher I/O counts and, critically, an order-of-magnitude shorter and less inductive path than a bond wire.

SI CONTEXT

Bump interconnects are ~50–100 µm tall, giving inductance in the tens of pH instead of nH. Controlled-impedance flip-chip routing (with ground bump shielding) supports multi-Gb/s to tens-of-Gb/s SerDes — the reason virtually all high-speed networking and compute ASICs use flip chip.

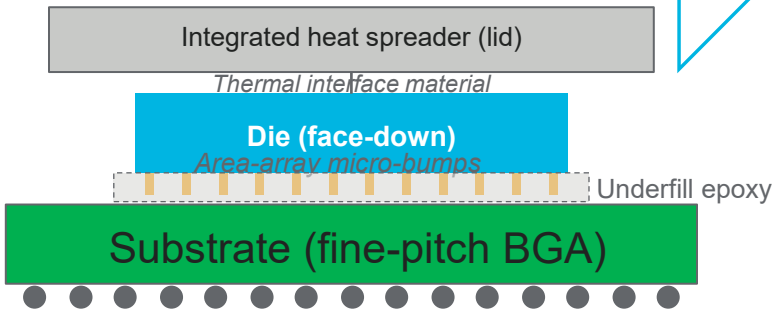
PI CONTEXT

Dense area-array power/ground bumps (not just perimeter) dramatically lower PDN inductance and spread current across many parallel paths, reducing IR drop and di/dt noise. This is what allows large die to source hundreds of amps without localized voltage droop.

10s of pH
Bump inductance

1,000s
I/O bumps per die

10–56+ Gb/s
Practical SerDes rates



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PACKAGE TYPE

Chiplets & Heterogeneous Multi-Die Integration

WHY IT EXISTS

Rather than one monolithic SoC, a product is composed of smaller "chiplet" die — compute, I/O, memory, network — each built on the process node best suited to its function, then reassembled in package. This is less a single package type than a design philosophy applied on top of 2.5D & 3D packaging platforms.

SI CONTEXT

Best connectivity for each application! Standardized die-to-die PHYs (e.g., UCIe, custom SerDes-based links) define controlled-impedance, closely-length-matched channels between chiplets so signal integrity is essentially the driver, not an afterthought — letting die from different vendors or nodes interoperate predictably.

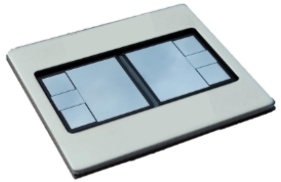
PI CONTEXT

Each chiplet brings its own power domain and decoupling needs; the package-level PDN must be co-designed across die boundaries so that switching noise in one chiplet (e.g., a digital compute die) doesn't couple into a sensitive neighbor (e.g., an analog/RF die).

UCIe
Emerging D2D standard

Mix nodes
Cost + performance lever

Reuse
Faster time-to-market

Marvell Training and Inference XPU	
Floorplan	
Interposer Size	3.4X (2 x 1.7X)
Substrate Size	87.5 x 72.5
Substrate stack-up	7-2-7
HBM	HBM3E
Status	HVM

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PACKAGE TYPE

2.5D Interposer

WHY IT EXISTS

Multiple die — typically a compute/logic die and one or more HBM memory stacks — sit side by side on a passive silicon (or organic) interposer with thousands of ultra-fine wires. The interposer, not the substrate, carries the highest-density die-to-die routing, then TSVs drop signals down to a conventional package substrate.

SI CONTEXT

Silicon interposer traces can be sub-2 µm pitch — 100x finer than substrate routing — enabling the thousand-plus-bit-wide HBM interface to run at low speed-per-pin with very low loss and tight length/skew matching across the whole bus.

PI CONTEXT

The interposer adds a low-loss power plane close to both die, but TSV vertical power delivery adds series resistance/inductance that must be modeled carefully. Decoupling capacitance is split between in-silicon and package-substrate embedded or SMT to cover different frequency ranges.

<2 µm
Interposer trace pitch

2048-bit+
HBM interface width

TSV
Vertical via technology

EMIB (Embedded Multi-Interconnect Bridge, CoWoS-L (Local Silicon Interconnect)

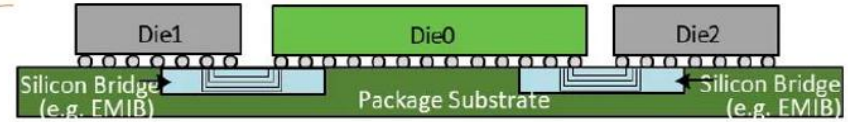


Photo credit: https://semiengineering.com/.

CoWoS-S (Silicon Interposer)

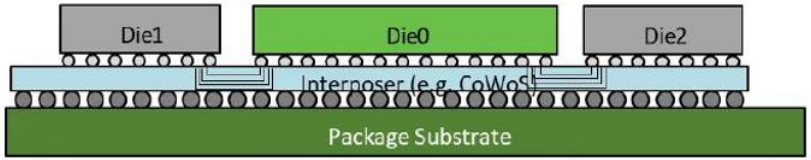


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CoWoS-R (RDL Interposer)

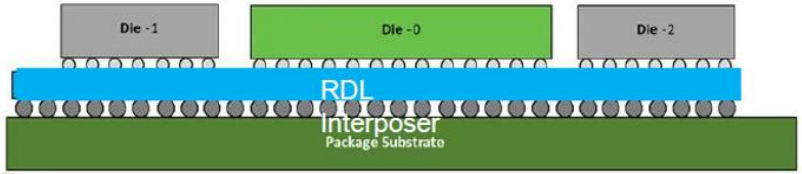
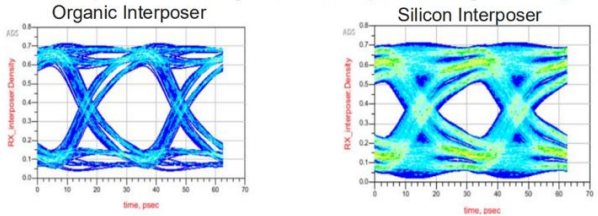


Photo credit: https://semiengineering.com/.

Silicon interposer has more jitter, loss compared to Organic interposer.



Silicon interposer can support higher routing density and better PDN decoupling.

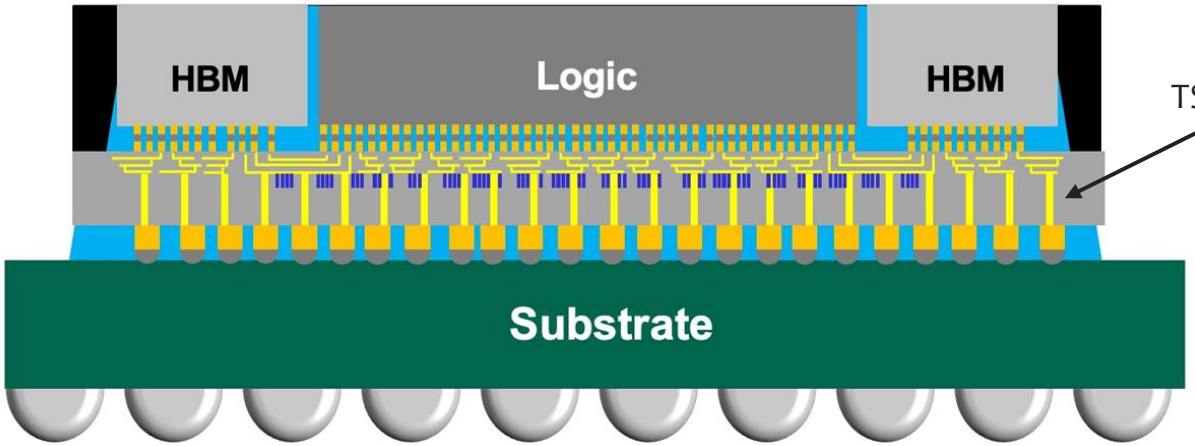
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CoWoS-S

Monolithic silicon interposer with through silicon vias (TSVs)

Monolithic silicon interposer = stiffness (CTE mismatch) = yield issues

Ready for production: 3.3X-reticle size (or ~2700mm^2) interposer



TSV (Through-Silicon Vias)

Photo credit: 3dfabric.tsmc.com

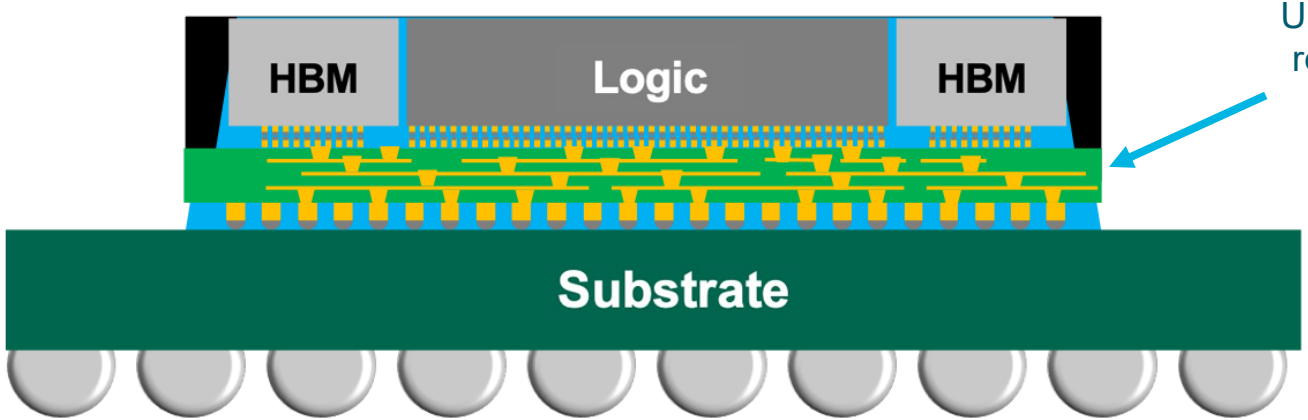
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CoWoS-R

Organic Interposer with fan-out RDL (redistribution layer) technology

↑ Reliability & Yield compared to CoWoS-S

The RDL interconnect offers good signal and power integrity with a lower RC value routing line to achieve a high data transmission rate.
The co-planar Ground-Signal-Ground-Signal-Ground (GSGSG) and interlayer ground shielding with 6 RDL interconnections offers superior electrical performance.



Up to 6 copper layers for routing with a minimum 4μm pitch (2μm line width/spacing)

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Photo credit: 3dfabric.tsmc.com

CoWoS-L

RDL Interposer with Local Silicon Interconnects (LSI)

- **High density routing where required,**

LSI allows high routing density die-to-die interconnect through silicon

Ability to integrate passive devices, such as stand-alone embedded deep trench capacitor die, underneath the SoC die to improve power management

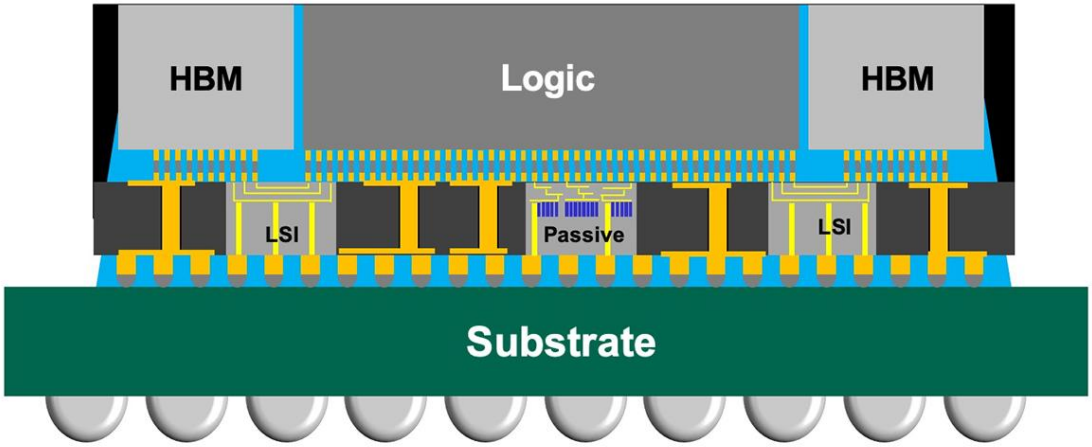


Photo credit: 3dfabric.tsmc.com

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PACKAGE TYPE

3D Stacking (TSV / Hybrid Bonding)

WHY IT EXISTS

Die are stacked directly on top of one another and connected vertically through TSVs or, in the newest hybrid-bonding processes, direct copper-to-copper bonds with no bumps at all. This shrinks the die-to-die path from millimeters to microns — the densest, shortest interconnect available.

SI CONTEXT

Vertical TSV/hybrid-bond links are extremely short (tens of µm) and low-capacitance, giving the lowest latency and highest bandwidth-per-mm² of any option — the basis for HBM cube stacking and cache-on-logic (3D V-Cache-style) designs where wide, short buses matter more than reach.

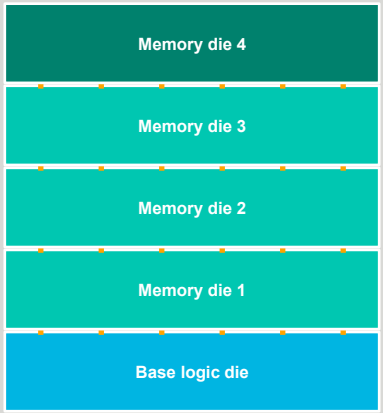
PI CONTEXT

Stacked die share a vertical power delivery network; every added tier increases current that must be delivered through the same TSV power pillars, raising the importance of low-resistance via arrays and dense on-die decoupling. Thermal stacking also raises local temperature, which itself affects PDN resistance and needs co-design with thermal solutions. SSN/Ground-bounce and di/dt major concerns

10s of µm	Highest	Thermal-limited
Vertical interconnect length	Interconnect density	Primary design constraint

HBM

TSV / hybrid-bond vertical vias between every tier



Up to 2K-bit wide data bus
Intense electrical & thermal constraints
Pin speeds beyond 12.8 Gbps
SI is primary bottleneck

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SI Comparison Across Package Types

Every package transition in history reduced one thing: the electrical length and discontinuity seen by a high-speed signal. The table below frames each package type by its dominant SI-limiting factor.

Package Type	Dominant Interconnect	Key SI Limiter	Typical Max Signaling
Wire Bond	Bond wire, 1–3 mm	Wire inductance / crosstalk	3–5 Gb/s
Flip Chip (FCBGA)	Micro-bump, 50–100 µm	Substrate via stubs, bump inductance	10–56+ Gb/s SerDes
Fan-Out WLP	RDL trace, few µm	RDL routing density / reach	Short-reach, high-density D2D
2.5D Interposer	Interposer trace, <2 µm	Crosstalk & IL at high density through Si	1000s of low-speed-per-pin bits (HBM)
3D Stacking	TSV / hybrid bond, µm-scale	Thermal + via density limits	~12Gbps per pin
Chiplets (D2D PHY)	Standardized D2D link (e.g., UCIe)	Cross-vendor channel matching	Multi-Gb/s per lane, many lanes

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PI Comparison Across Package Types

Power delivery network (PDN) quality — from DC (IR drop, Current density) to transient / time-domain response, and Simultaneous Switching Noise (ground bounce) — is just as dependent on package architecture as signal routing. Denser, shorter interconnects generally mean lower PDN inductance but tighter thermal and current-density limits. di/dt inrush current, noise coupling and

Package Type	Power/Gnd Path	Key PI Concern	Mitigation Strategy
Wire Bond	Perimeter bond wires	High loop inductance, SSN	Multiple parallel P/G wires, on-board decoupling
Flip Chip (FCBGA)	Area-array bumps	IR drop under large die	Dense bump grid, package + die-side decoupling
Fan-Out WLP	Thin-film RDL planes	Limited bulk decoupling room	On-die caps, tight P/G plane coupling
2.5D Interposer	TSV power pillars	TSV resistance/inductance	Wide TSV arrays, multi-tier decoupling
3D Stacking	Shared vertical TSVs	Current scales with tier count	Low-R via arrays, thermal-aware PDN co-design
Chiplets	Per-die domains + shared rails	Cross-die noise coupling, PHY req’ts	Domain isolation, guard rails, local decoupling

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Packaging Technology Challenges

Technical

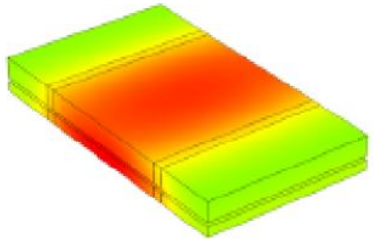
- Signal integrity
- Large module warpage
- Power delivery
- Hot spot mitigation
- 3D heat transfer
- Supplier capability and readiness

Business

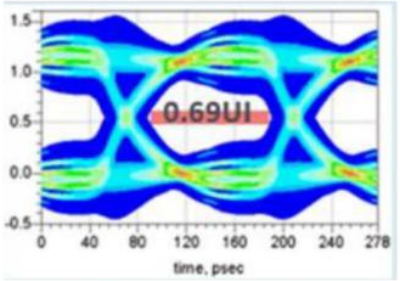
- Capacity
- Cycle time
- Supply chain
- Cost



Module Warpage.



Thermal simulation: SoC heating HBMs.



Signal Eye Diagram

Marvell must deliver leading-edge packaging solutions for our clients.

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Chart: S. Donovan

APPLIED AT MARVELL

Advanced Packaging in Marvell Data Center Group

Marvell's custom silicon and data infrastructure products — electro-optics, switching, storage, and compute-adjacent ASICs — sit squarely in the regime where package choice determines whether a design hits its bandwidth, power, and cost targets.

Custom Compute & ASIC Platforms

Chiplet-based construction lets a compute die, SerDes/I/O die, and memory be mixed and matched across customer programs — applying the D2D and PDN co-design principles covered above.

High-Bandwidth Memory Interfaces

2.5D interposer integration brings HBM adjacent to logic with the fine-pitch, low-loss routing needed to hit multi-TB/s memory bandwidth at acceptable power.

High-Speed SerDes & Networking ASICs

Flip-chip FCBGA remains the backbone for switch and PHY silicon, where controlled-impedance bump routing supports 200+ Gb/s per lane.

Co-Packaged Optics & Electro-Optics

Multi-die, heterogeneous packaging brings optical engines electrically close to switch silicon, cutting the copper reach that otherwise limits SI at high baud rates.

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KEY TAKEAWAYS

1. Packaging history is a tale of shrinking parasitic inductance & capacitance to keep pace with rising I/O speed and signal count.

2. Each package type — wire bond, flip chip, fan-out, 2.5D, 3D, chiplets — exists to solve a specific bandwidth, density, cost, or power problem, not to replace all others.

3. SI and PI are not afterthoughts: bump/via/wire parasitics and PDN topology are first-order inputs to package architecture and product design.

4. Marvell’s custom silicon and infrastructure products draw on this full menu, matching package architecture to each product's bandwidth and power profile.

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Thank You

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Q&A



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